REMARKS

Claims 1-11 are pending in the application. All claims were rejected.

All claims have been amended to conform to U.S. practice, and in several cases to clarify the claimed structures. While a "clean" copy of the claims is no longer required, because of the extensive amendments above and for the convenience of the Examiner, a clean copy of the current state of all claims is attached as an Appendix.

According to the Examiner's requirement, Figures 1-3 have been amended to add a "prior art" label.

35 U.S.C. § 112(1) – Enablement

Claims 7-8 were rejected as non-enabled by the specification. The Examiner specifically states that the operation of the circuits illustrated by Figures 5 and 6, and their interrelation to the circuit shown in Figure 4 "is not understood." Applicant respectfully notes that while the specification text does not specifically describe each element and their interconnections, these are shown clearly in the figures as to be understood by one of skill in the art. The specification does describe in detail the inputs, outputs, and operation of the circuits of Figures 5 and 6, including relevant formulae, e.g., in paragraphs 0044-0050.

Figures 5 and 6, and claims 7 and 8, are therefore believed to be fully enabled, and these rejections are traversed.

35 U.S.C. § 112(2) – Definiteness

All claims have been amended to conform to U.S. practice, and where appropriate, to clarify the claimed circuit structures. All claims are now believed to be clear and definite, and to particularly point out and distinctly claim the subject matter which the Applicant regards as his invention. All §112(2) rejections are therefore believed to become.

All §112(2) rejections are traversed.

35 U.S.C. § 101 – Double Patenting

The Examiner's provisional double patenting rejection has been noted. This issue will be addressed when one of the subject patents has been issued, and the issued claims can be analyzed and distinguished.

35 U.S.C. § 102 – Anticipation

Claims 1-6 and 11 have been rejected as anticipated by Ishihara (USP 6,054,883). The Examiner correctly notes that some elements of Ishihara appear to be similar to elements of claim 1. Claim 1, and amended claim 11, require that the splitting means also have the characteristics of an "all-pass," which the specification describes as a circuit that "produces two quadrature signals with equal amplitudes and the gm/C time constant of an all-pass tracks the oscillation frequency (using the same tuning mechanism) of the input signal outputted by the oscillator".

Nothing in Ishihara appears to teach or suggest this feature. If the Examiner believes this

feature is present in Ishihara, he is respectfully requested to specifically point it out.

As an anticipation reference must teach EVERY aspect of the claims, and Ishihara does not, Ishihara fails to anticipate claims 1-6 and 11.

The anticipation rejections are traversed.

35 U.S.C. § 103(a) – Obviousness

Claims 7, 9, and 10 were rejected as obvious over Ishihara in view if Liu (USP 6,496,545). Applicant notes that no proper motivation to combine the Ishihara and Liu references has been stated. While both Ishihara and Liu incorporate phase shifters, Liu is directed toward a side-band mixer, and there is no indication that one designing a phase shifter, or even a phase shifter with error detection, would look to a side-band mixer patent for any teachings.

The stated motivation to combine is "for the expected advantage of increased sideband rejection." As the Examiner is surely aware, a proper motivation must be one that would motivate one of skill in the art of the primary reference, Ishihara, to look to the secondary reference, Liu, for teachings. Nothing in Ishihara teaches or suggests that "increased sideband rejection" is desirable, and in fact, sideband rejections is not mentioned at all in Ishihara.

As no proper motivation to modify/combine has been stated, a *prima facie* obviousness rejection has not been made, and all obviousness rejections are traversed.

All rejections stated in the Office Action mailed 04/23/03 have been traversed.

SUMMARY

For the reasons given above, the Applicants respectfully request reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: July 22, 2003

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APPENDIX

Clean Version of Claims as Currently Amended

1. A tunable quadrature phase shifter, comprising:

an input means for inputting an input signal;

splitting means for splitting the input signal into two essentially orthogonal first and second signals;

adding means for adding said first and second signals;

subtracting means for subtracting said first and second signals;

a first output for outputting a first output signal based on the output signal from said adding means; and

a second output for outputting a second output signal based on the output signal from said subtracting means, wherein said splitting means is an all-pass.

2. The phase shifter of claim 1, further comprising a first output buffer means for buffering said first output signal, and a second output buffer means for buffering said second output signal.

3. The phase shifter of claim 1, further comprising a first transimpedance converter having its input connected to said input means.

4. The phase shifter of claim 1, further comprising a first transimpedance converter having its output connected to said first output, and a ~~third~~ second transimpedance converter having its output connected to said second output.

5. The phase shifter of claim 3, wherein the transimpedance converter is a transimpedance amplifier.

6. The phase shifter of claim 2, wherein said first and second output buffer means are first and second transimpedance converters, respectively.

7. The phase shifter of claim 1, the splitting means comprising at least a first transistor with its collector connected to its base and its emitter coupled to a predetermined potential, a second transistor with its base connected to the base of said first transistor and its emitter coupled to said predetermined fixed potential, and a capacitor coupled between the junction of the bases of said first and second transistor and said predetermined potential.

8. The phase shifter of claim 1, the splitting means comprising:

a first input for inputting an input signal;

a second input for inputting an inverse input signal;

a first transistor with its collector connected to its base and its emitter coupled to a predetermined potential;

a second transistor with its base connected to the base of said first transistor and its emitter coupled to said predetermined potential;

a third transistor with its collector connected to its base and its emitter coupled to a predetermined potential;

a fourth transistor with its base connected to the base of said third transistor and its collector coupled to said predetermined potential; and

a capacitor coupled between a first junction of the bases of said first and second transistors and a second junction of the bases of said third and fourth transistors.

9. The phase shifter of claim 7, wherein said transistors are npn transistors.

10. The phase shifter of claim 7, wherein said predetermined potential is zero.

11. A data and clock recovery unit comprising a phase detector which includes a phase shifter having

an input means for inputting an input signal;

splitting means for splitting the input signal into two essentially orthogonal first and second signals;

adding means for adding said first and second signals;

subtracting means for subtracting said first and second signals;

a first output for outputting a first output signal based on the output signal from said adding means; and

a second output for outputting a second output signal based on the output signal from said subtracting means, wherein said splitting means is an all-pass.